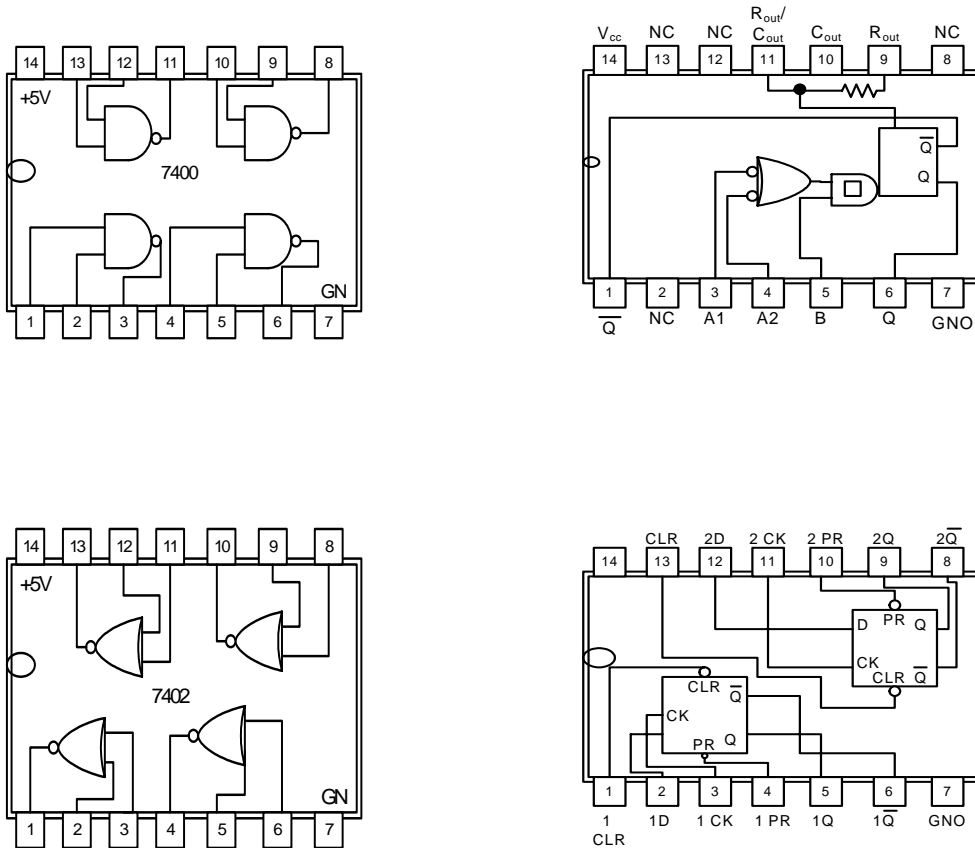


## PHYSICS 536

### Experiment 14: Basic Logic Circuits

Several T<sup>2</sup>L ICs will be used to illustrate basic logic functions. Their pin connections are shown in the following sketch, which is a top view.



Pin 14 ( $V_{cc}$ ) is connected to +5V and pin 7 is connected to ground for all of these ICs. Be certain that the power supply voltage is +5V **before** it is applied to IC because a higher voltage will destroy the IC. AN unconnected T<sup>2</sup>L input is held high internally. Short lengths of #22 wire should be used for connections. A notch and/or a small circle near pin 1 indicates the pin orientation. Insert a short, bare wire in the board sockets as a connection point for the scope probe or meter. (The pointed meter probe will damage a socket if it is inserted directly.) Accidental damage to the IC pins is common. Use a small screwdriver to remove the IC from the sockets or hold it at the ends.

### GRADING

A form is provided at the back of these instructions so that your observations can be recorded simply. The completed form is your lab report. Give it to your instructor at the end of the period. **No further laboratory report is required.**

**A. Univibrator.** A univibrator produced a rectangular pulse whose width is controlled by the time required to charge a capacitor. Connect the 74121-univibrator IC as shown in the sketch.

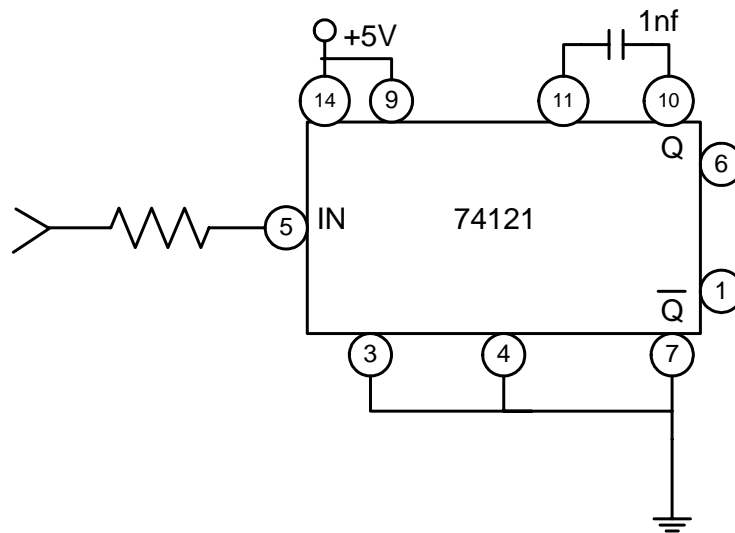


Figure 1

Position the IC on the left side of the plug-in board so that other ICs can be added later. The 1nf external timing capacitor is charged by current flowing through a resistor inside the IC. The input signal should be a **square wave**. The univibrator is triggered by the positive edge of the square wave. A 1K resistor is included in series with  $v_i$  to protect the input of the IC when the square wave goes negative. (Normal T<sup>2</sup>L signals are in the 0 to +5V range.)  $v_i$  should be connected to the circuit and the external trigger of the scope. Set the scope to respond to an external trigger. Set the signal generator to produce a 100kHz square wave with maximum amplitude. Observe  $v_i$  with one of the input channels, and set the trigger slope and level so that the scope triggers on the positive edge of the square wave. Reduce the amplitude of the square wave to approximately 7V(p-p). The vertical input of the scope should be set for DC coupling so that you can tell if a signal is in the high or low state when it is not changing. Ground the inputs and set the traces on convenient horizontal lines so that you will know the vertical positions of 0V. You will usually be observing two signals simultaneously. You may use scope probes or cables.

**1) Homework** Continue to use external triggering. Observe Q and  $\overline{Q}$  with a sweep of 0.5μsec/div.

A sketch of the  $v_i$ , Q, and  $\overline{Q}$  are shown at the beginning of the report form as an illustration. The 1nf capacitor should provide a pulse width between 1 and 2 μsec. The standard T<sup>2</sup>L levels are 0V and 3.5V. Compare your waveforms to the report sketch.

Move one probe from  $\overline{Q}$  to  $v_i$  so that you can observe the time relationship between  $v_i$  and  $Q$ .

Continue to observe  $v_i$  and  $Q$ . Change the horizontal sweep to  $10\mu\text{sec/div}$ .  $Q$  should be a sequence of pulses, which at  $10\mu\text{sec}$  apart. Vary the square wave frequency and the horizontal sweep speed to be sure that you understand the display. You also may vary the square wave amplitude. The univibrator should trigger correctly when the amplitude is between 3V and 10V. Leave the amplitude at 7V. Reset the sweep to  $0.5\mu\text{sec/div}$  and do not change it until step 17.

Be sure that these waveforms are correct before you proceed because you will be using the pulses from this univibrator as the input signal for several other circuits.

## B. NAND Gates.

The outputs of the univibrator will be connected to the two inputs of the NAND gate. A second NAND gate is used as inverter. Use two gates in one 7400 IC. The inverter may be connected at the beginning, but it won't be used until step 6. Don't forget to connect +5V to pin-14 and ground pin-7.

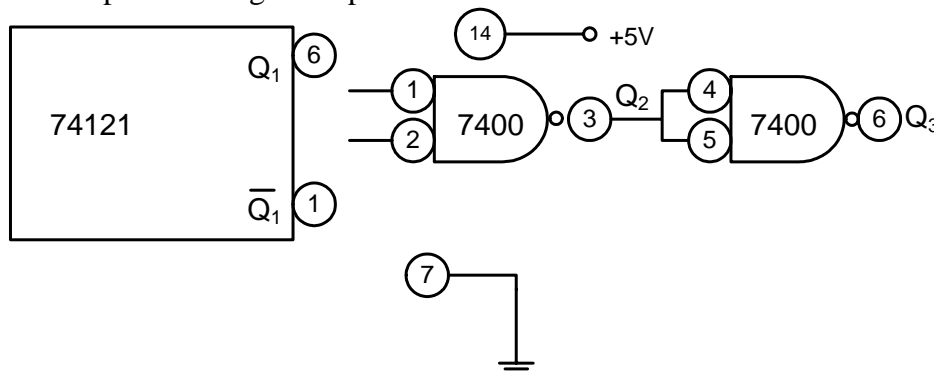


Figure 2

**2) Homework** Connect  $Q_1$  to A and connect B to ground. Is  $Q_2$  switching between high and low states or does it stay in one of them? (A blank space is provided for your answer on the report sheet.)

**3) Homework** Change the input B connection to +5V. Observe and sketch the signal at A and  $Q_2$  in the space provided on the report sheet.

**4) Homework** Remove the connection from input B. (B is connected to nothing in this step.) Observe  $Q_2$ . A sketch is not necessary. Briefly explain what you see by comparison to step 3.

**5) Homework** Connect  $Q_1$  to A and B. \* Observe A-B and  $Q_2$ . Compare  $Q_2$  to one of the preceding steps. A new sketch is not needed.

**6) Homework** Continue with  $Q_1$  connected to A and B. Observe and sketch A-B and  $Q_3$ . What is the name of the logic function provided by this combination?

**7) Homework** Connect  $\overline{Q_1}$  to A and +5V to B. Observe and sketch A and Q<sub>2</sub>. (Q<sub>2</sub> would be the same if the roles of A and B were reversed.) This step illustrates de Morgan's law. A NAND for high level is an OR for low level.

**8) Homework** Leave  $\overline{Q_1}$  connected to A. Connect ground to B. Observe Q<sub>2</sub> and explain by comparison to step 7.

\*Consider this an illustration of separate pulses arriving at A and B at the same time.

### C. NOR Gates.

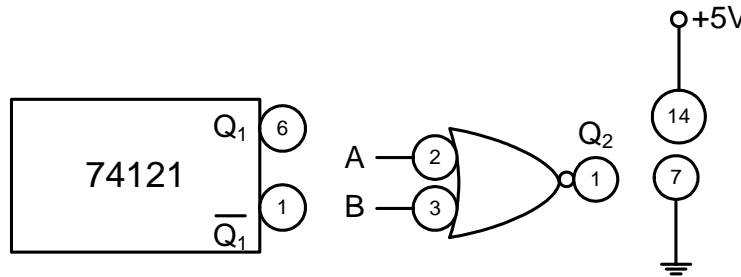


Figure 3

**9) Homework** Connect Q<sub>1</sub> to A and ground to B. Observe and sketch A and Q<sub>2</sub>. Q<sub>2</sub> would be the same if the roles of A and B were reversed.

**10) Homework** Change B to +5V. Observe Q<sub>2</sub> and explain by comparison to step 9.

**11) Homework** Connect  $\overline{Q_1}$  to A and B. Observe A-B and Q<sub>2</sub>. This is a second illustration of de Morgan's law. A NOR gate becomes an AND gate for low inputs. (You may move A or B from  $\overline{Q_1}$  to +5V to see that this prevents Q<sub>2</sub> from going positive.)

### D. Logic Circuit Illustrations.

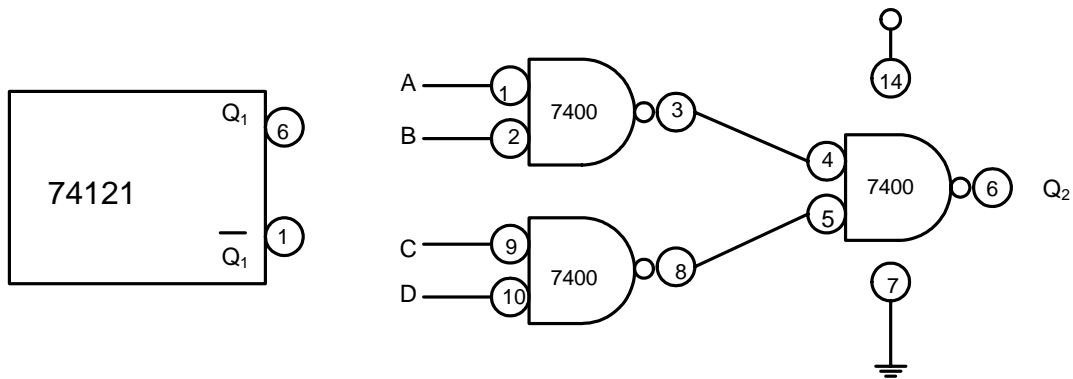


Figure 4

**12) Homework** Write the logic equation that specifies  $Q_2$  as a function of A, B, C, and D. (Hint: apply de Morgan's law to the gate on the right.)

**13) Homework** Connect  $Q_1$  to A and B. Connect C and D to ground. Observe and sketch A-B and  $Q_2$ .  $Q_2$  would be the same if you reversed the roles of A-B and C-D. Do your observations confirm your logic equation in step 12?

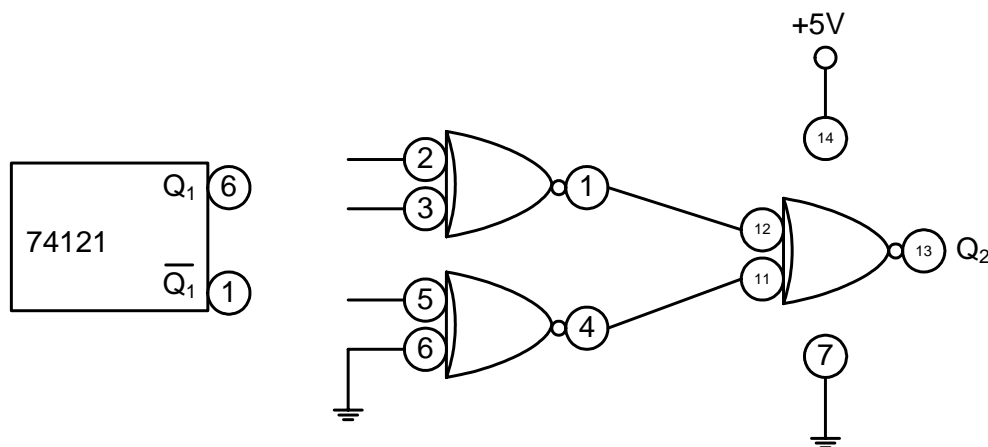


Figure 5

**14) Homework** Again the function should be evident when you apply de Morgans law to one of the gates. Write the logic equation which specifies Q as a function of A, B, C, and D.

**15) Homework** Connect  $Q_1$  to A and C. Connect B and D to ground. Observe and sketch A-C and  $Q_2$ . Then move C to ground and observe  $Q_2$ . Do your observations confirm you logic equation from step 14?

### E. Binaries.

The two NAND gates in the following circuit are "cross coupled" to form a set-reset binary that responds to low levels at the input.

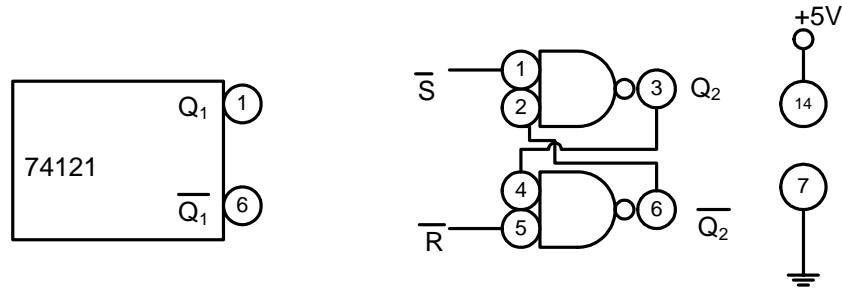


Figure 6

Observe  $Q_2$  and  $\overline{Q_2}$  with the scope. One will be high and the other low. Initially the  $\overline{S}$  and  $\overline{R}$  inputs are not connected. Remember that these inputs are held high internally. Connect a wire to ground and touch it to  $\overline{S}$  (if  $Q_2$  low) to  $\overline{R}$  (if  $Q_2$  is high). The binary should change state each time it receives the appropriate low input level.

**16) Homework** Connect  $\overline{Q_1}$  to  $\overline{S}$  and  $Q_1$  to  $\overline{R}$ . Observe and sketch  $Q_1$  and  $Q_2$ . The type-D binary in the next circuit is connected as a “flip-flop”.

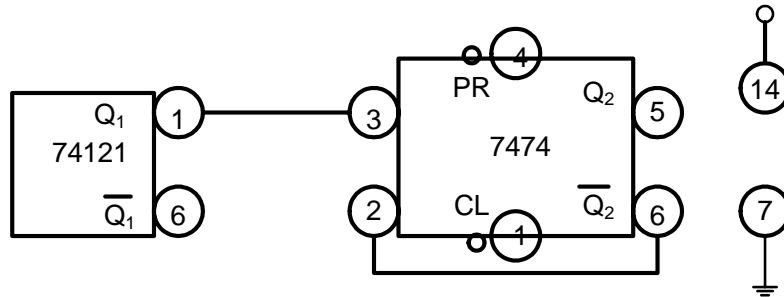


Figure 7

**17) Homework** Use a horizontal sweep of  $5\mu\text{sec/div}$ . Observe and sketch  $Q_1$  and  $Q_2$ . Use **internal trigger (positive slope) from the channel that is observing  $Q_2$** . If you trigger from  $Q_1$ , the trace showing  $Q_2$  can start either high or low, which is confusing.

**18) Homework** Continue to observe  $Q_1$  and  $Q_2$ . Connect a wire from ground to the “preset” input (PR). Describe  $Q_2$ . Move the ground wire to the “clear” input (CL). Describe  $Q_2$ .

A second flip-flop (from the same 7474 IC) is added in the next circuit. The two flip-flops form a scale of 4 binary counter, i.e.  $Q_3$  will return to its original state after four pulses from  $Q_1$ .

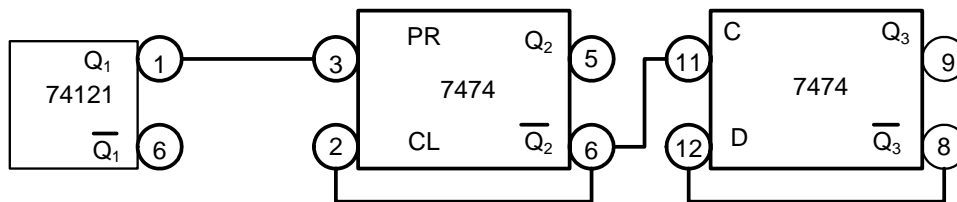
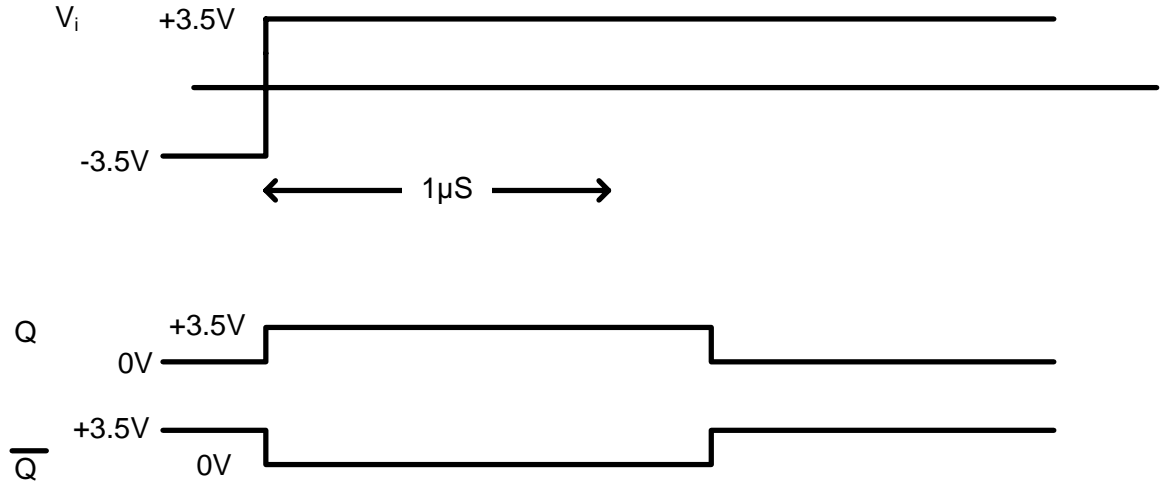


Figure 8

**19) Homework** Use  $10\mu\text{sec/div}$  sweep. Observe  $Q_1$  and  $Q_2$ , triggering internally from the positive slope of  $Q_2$ . Observe  $Q_2$  and  $Q_3$ , triggering internally from the positive slope of  $Q_3$ . Sketch  $Q_1$ ,  $Q_2$ , and  $Q_3$ .

**PHYSICS 536**  
**Report for Experiment 16**

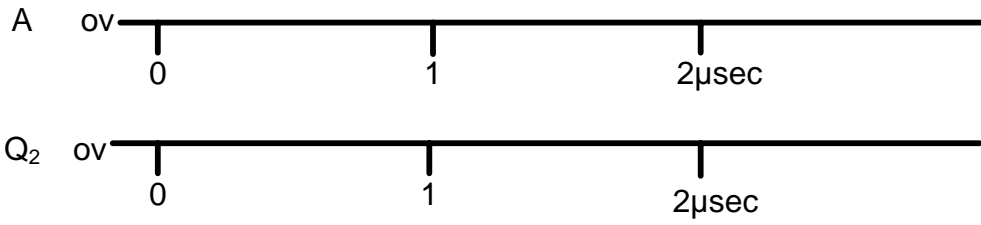
1)



2)



3)



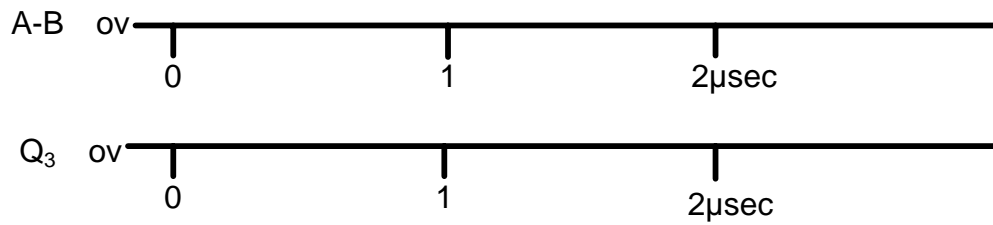
4)



5)



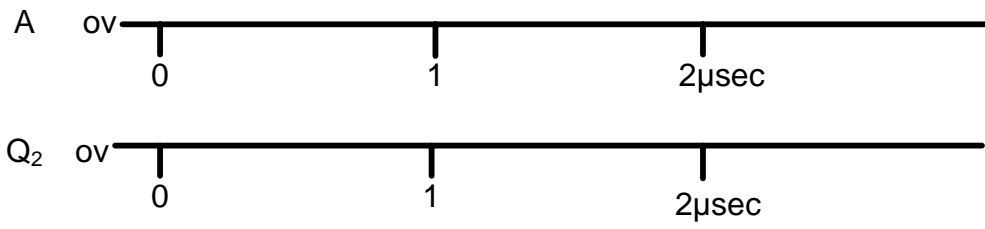
6)



NAME \_\_\_\_\_



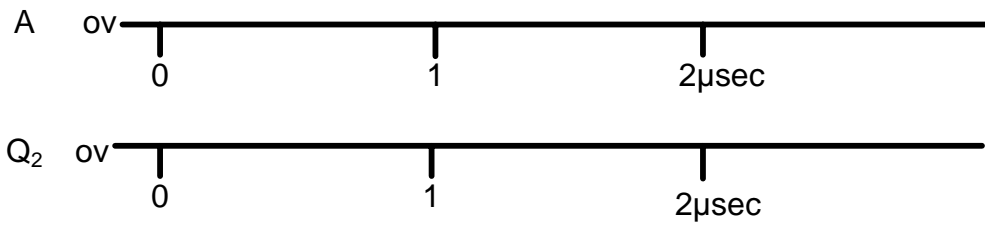
7)



8)



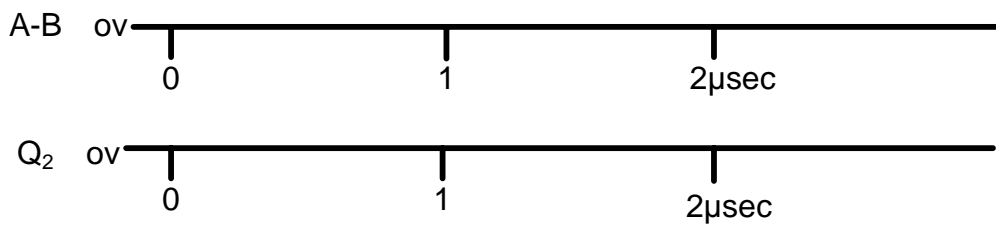
9)



10)



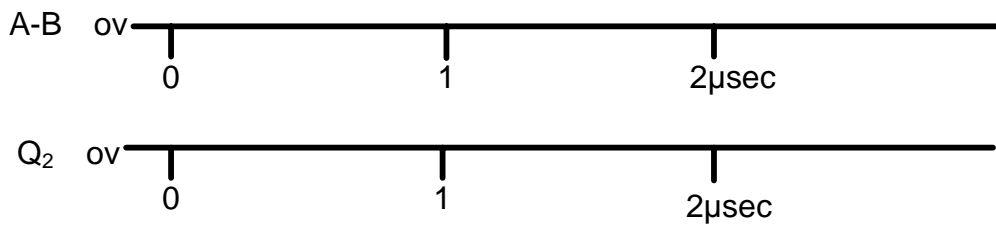
11)



12)



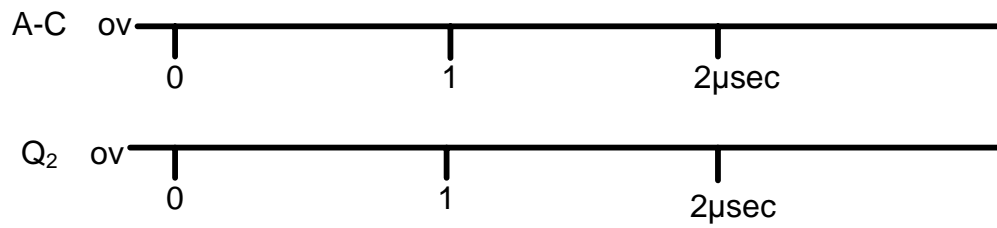
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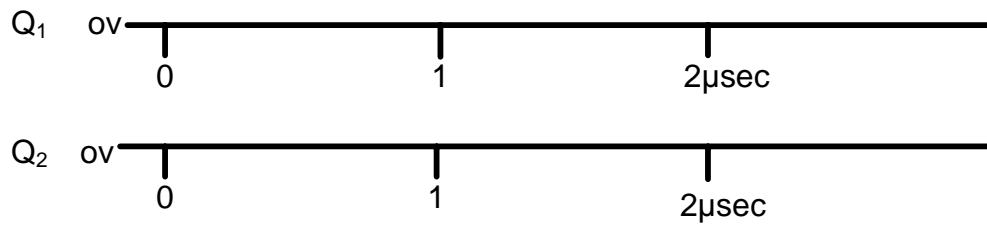
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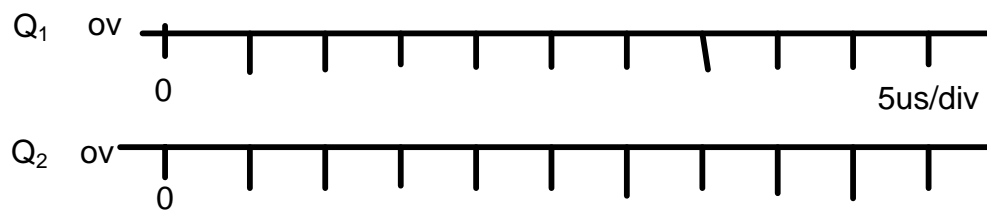
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16)



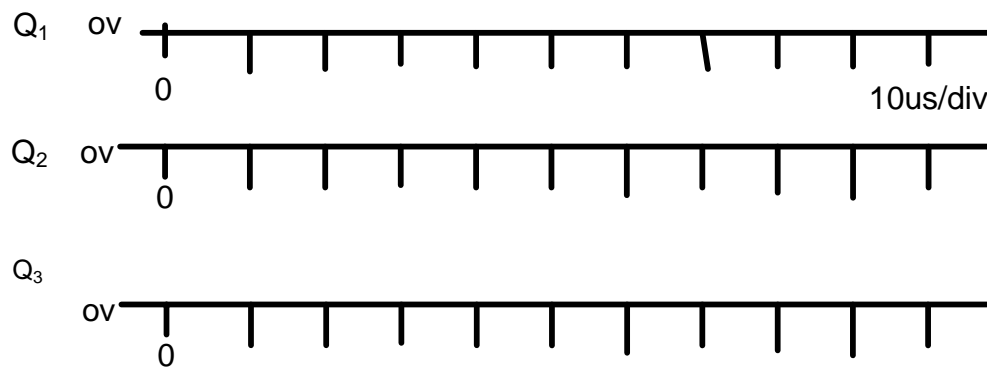
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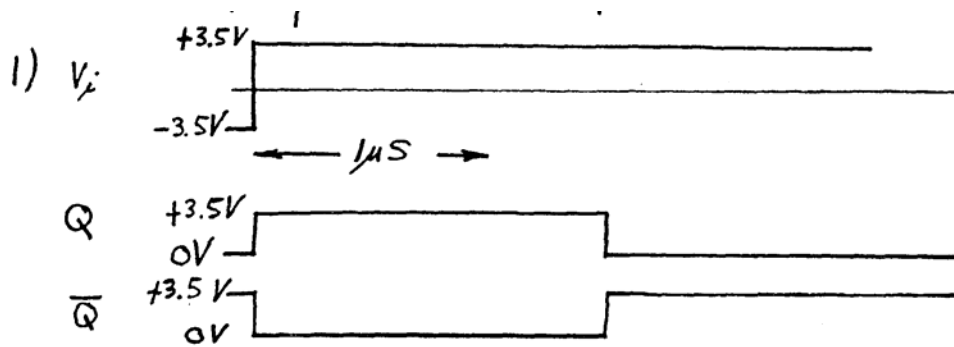


18)

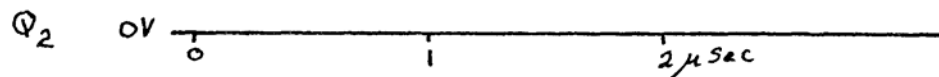
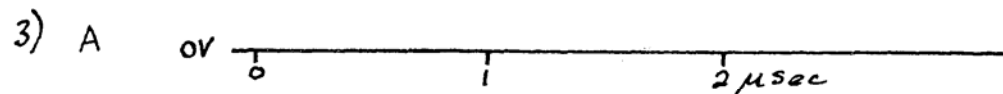
PR ACTIVE: \_\_\_\_\_  
CL ACTIVE: \_\_\_\_\_

19)



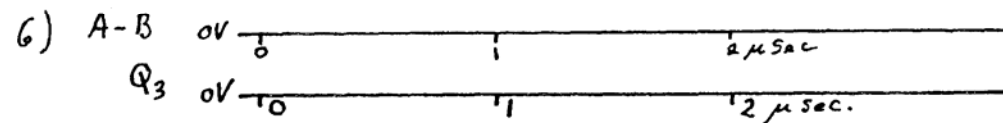


2) \_\_\_\_\_

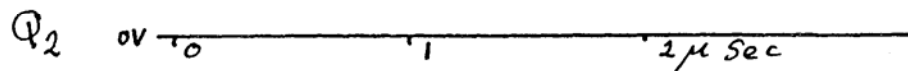
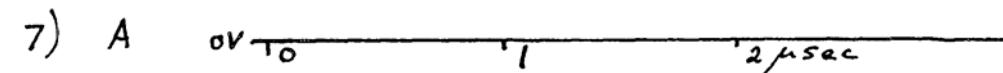


4) \_\_\_\_\_

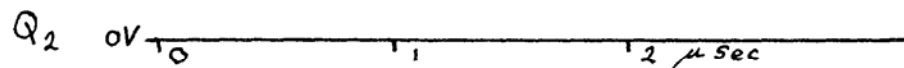
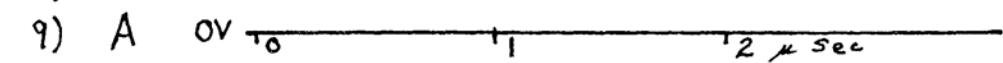
5) \_\_\_\_\_



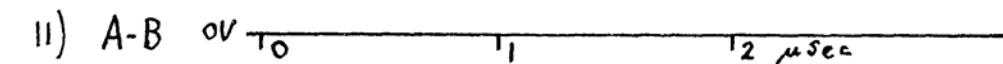
Name: \_\_\_\_\_



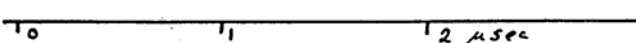
8) \_\_\_\_\_

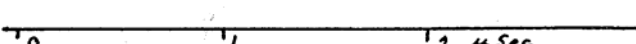


10) \_\_\_\_\_



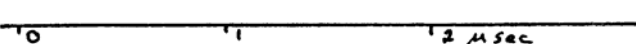
12)  $Q =$  \_\_\_\_\_

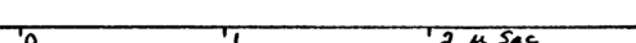
13) A-B 0V  2  $\mu$ Sec

$Q_2$  0V  2  $\mu$ Sec

Logic Eq. Confirmed? \_\_\_\_\_

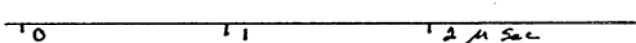
14)  $Q =$  \_\_\_\_\_

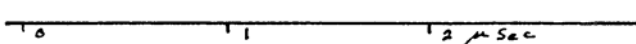
15) A-C 0V  2  $\mu$ Sec

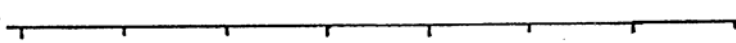
$Q_2$  0V  2  $\mu$ Sec


Describe  $Q_1$  when C is low: \_\_\_\_\_

Logic Eq. Confirmed? \_\_\_\_\_

16)  $Q_1$  0V  2  $\mu$ Sec


$Q_2$  0V  2  $\mu$ Sec

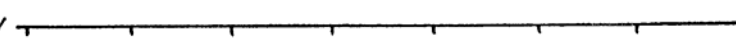
17)  $Q_1$  0V  5  $\mu$ S/div

$Q_2$  0V 

18) PR ACTIVE: \_\_\_\_\_

CL ACTIVE: \_\_\_\_\_

19)  $Q_1$  0V  10  $\mu$ S/div

$Q_2$  0V 

$Q_3$  0V 